CoaXPress 2.1 Host IP Core

1-Lane CXP-12 Host Controller for AMD FPGAs

The ApotheoTech CoaXPress Host IP Core provides a complete, low-resource CoaXPress 2.1 host implementation for high-speed machine vision applications. Supporting 1-lane CXP-12 operation at up to 12.5 Gbps aggregate bandwidth, this IP enables direct camera connectivity with a simple AXI4-Stream video output interface.

Key Features

- CoaXPress 2.1 compliant
- 1-lane CXP-12 (up to 12.5 Gbps)
- 8, 10, 12, and 16-bit pixel formats
- Hardware trigger generation
- Camera register access (GenICam)
- AXI4-Stream video output
- AXI4-Lite control interface
- Low resource footprint

Specifications

Standard	CoaXPress 2.1
Lanes	1
Downlink	12.5 Gbps/lane, 8b/10b
Max Bandwidth	12.5 Gbps
Uplink	41.66/20.83 Mbps, 8b/10b

Hardware Requirements

The CoaXPress physical layer requires an external equalizer/driver IC to interface the FPGA's GTH/GTY transceivers with the 75Ω coaxial cable. This IC handles signal conditioning, cable equalization, and the bidirectional high-speed/low-speed multiplexing required by CXP-12.

ApotheoTech FMC Interface Cards

For rapid development and evaluation, ApotheoTech offers FMC interface cards with integrated equalization, providing a complete hardware solution:

Part Number	Description	Use With
APT-C11-FMC	Single-lane CXP-12 FMC, supports both Host and Device modes. Ideal for single-camera applications or device IP development.	ZCU106, KCU116, other FMC carriers
APT-C40-FMC	Quad-lane CXP-12 FMC, 4 independent Host channels. For multi-camera systems or high-bandwidth aggregation.	ZCU106, KCU116, other FMC carriers

The APT-C11-FMC is purpose-built for the ApotheoTech CoaXPress Host and Device IP cores and provides the hardware for the loopback and example designs described below. The card and its example designs target AMD (Xilinx) architectures only. Contact us for details on third-party equalizer IC integration.

Supported CXP 2.1 Features

The CoaXPress 2.1 Host IP Core implements all CXP 2.1 features specified in the Japanese Industrial Imaging Association's CoaXPress Version 2.1 document save for:

Section	Feature	Support	Details
4.4	Connection Aggregation	No	Support only 1 connection
10.4.1	Pixel Types	Limited	Only supports RGB, YUV, Mono, and Bayer image formats
10.4.2	Pixel Packing	Limited	Supports only, 8, 10, 12, 16 bits
10.4.5	Tap Concept	Limited	Supports 1X-1Y (default line scan)
10.5	GenDC Streams	No	GenDC Streams are not supported.
11	Link Sharing	No	Link Sharing is not supported

For pixel types and packaging, the encrypted core will be compiled upon request. For unsupported features, they may be integrated to the core with an NRE.

Target Applications

The CoaXPress Host IP is ideal for systems requiring high-bandwidth camera connectivity with deterministic, low-latency video capture:

- Industrial inspection
- Print inspection
- Scientific imaging
- Semiconductor metrology
- Medical imaging
- High-speed capture

Supported FPGA Families

The CoaXPress Host IP Core is available for AMD (Xilinx) FPGA families with GTH or GTY transceivers capable of 12.5 Gbps operation. Pre-validated targets include Zynq UltraScale+ MPSoC. Other FPGA families can be supported with NRE engagement.

Resource Utilization (Zynq UltraScale+)

Configuration	Bandwidth	LUTs	Registers	BRAM
1-Lane CXP-12	12.5 Gbps	5592	7309	6.5

Resource usage excludes GT transceivers and user logic. Results from Vivado 2024.2. Other FPGA families available with NRE.

Evaluation & Demo Bitstreams

A pre-built demonstration bitstream is available for the ZCU106, allowing immediate validation of the CoaXPress link before committing to a full design.

Available Demo Configurations

Board	FMC Card	Video Output	Description
ZCU106	APT-C11-FMC	DisplayPort	Host and Device cores running in loopback over a single APT-C11-FMC, with live DisplayPort output. This is the standard test bitstream for the core on the ZCU106.

Demo bitstreams require APT-C11-FMC or compatible FMC card. Bitstream is available only. For design files, please contact ApotheoTech for pricing.

Example Designs

Complete, synthesizable example designs are available to accelerate your integration. Each example design includes full RTL source, constraints, and a Vivado project configured for the target board and APT-C11-FMC interface card.

Available Example Designs

Example Design	Description	Availability
Basic Streaming	CoaXPress 2.1 Host IP with AXI4-Stream output to frame buffer. Trigger control and status monitoring via UART. ZCU106 + APT-C11-FMC.	Included
DisplayPort Loopback	Host IP receiving from the ApotheoTech Device IP on the same board, with live DisplayPort output for end-to-end validation without a camera. Requires a license for both cores. ZCU106 + APT-C11-FMC.	Free with both cores
PCIe DMA + Sample Application	PCIe DMA engine with a sample Linux application and driver. Full control of the Host IP over PCIe, including camera register access and frame transfer. KCU116 or ZCU106 + APT-C11-FMC.	Paid add-on
Custom Integration	Work directly with ApotheoTech to develop a custom design for your requirements and target platform.	NRE

Deliverables

IP Core	Encrypted netlist for target FPGA family
Integration Guide	Complete signal descriptions, register map, timing diagrams, integration guidelines
Instantiation Templates	Verilog and VHDL wrapper templates
Example Designs	Complete Vivado projects with RTL source and constraints
Technical Support	Email support included with license, premium support available

Licensing & Delivery

Both cores present AXI4-Lite control and AXI4-Stream data interfaces, and are delivered as an encrypted netlist compiled for a targeted GTY, GTH, or GTP transceiver configuration. Each license includes one year of updates. After that period, a license renewal is required to make changes to the core.

License Configurations

Configuration	Includes	Intended For
Host Only	CoaXPress 2.1 Host IP with AXI4-Stream video output.	Frame grabbers and capture cards
Host + Test Device	Host IP, plus a Device IP restricted to an internal test pattern generator with no AXI4-Stream video input. Priced below the full Device core, and gives you a link partner for bring-up and regression testing.	Capture card development
Device Only	CoaXPress 2.1 Device IP with AXI4-Stream video input.	Embedded cameras and image sources
Host + Device	Both cores at full feature set, plus the DisplayPort loopback example design.	End-to-end camera and grabber systems

Contact & Ordering

For pricing, evaluation access, or technical questions, contact ApotheoTech:

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